REMARKS/ARGUMENTS

The Applicants hereby respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks/arguments. Claims 1-20 were originally filed in the present application. By the present Amendment, claims 1 and 11 are amended. New claims 21 and 22 have been added, but no new matter has been added and no claims have been canceled. Accordingly, claims 1-22 are now pending in the present application.

I. SPECIFICATION

The Office Action has objected to the specification, namely, the title of the application as not being descriptive. In response, the Applicants have replaced the title of the application.

II. REJECTIONS UNDER 37 C.F.R. §102

The Office Action has rejected claims 1, 4, 6-7, 9-11, 14, 16-17 and 19-20 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,646,545 to Trimberger *et al.* In response, the Applicants have amended independent claim 1 to recite, among other things, that (1) the configuration data modules are "to be retrieved *from outside the logic computing system*," and (2) that the "logic computing unit provides a logical function value of logic input data as logic output data, by referring to at least one configuration data module retrieved and stored in at least one of said plurality of data storage units (41a to 41d, 49a to 49d) *while another of said plurality of configuration data modules is being retrieved from outside the logic computing unit and stored in another one of said data storage units* (41a to 41d, 49a to 49d)." In addition, independent claim 11 has been similarly amended.

In contrast, Trimberger does not disclose these elements. In conventional FPGAs, configuration memory cells are coupled to configurable logic blocks (CLBs) to

specify the function to be performed by each CLB, as well as to the configurable routing structure to specify the coupling of the input and output lines of each CLB. Trimberger discloses an FPGA that replaces the basic 5 transistor memory cells, which control the logic function in a conventional FPGA, with a bit set having multiple memory cells (8 in the preferred embodiment). These additional configuration memory cells are used to increase the logic density of the FPGA by providing a distinct bit set for each prior FPGA programming point. Thus, by providing "n" memory cells in place of each prior single 5T memory cell, Trimberger provides n-times the amount of logic than found in conventional FPGAs. (Col. 6, lns. 36-63). Accordingly, as stated in Trimberger:

> By reconfiguring the CLBs, the number of function generators in the CLB, typically conventional look up tables ("real LUTs"), needed to implement a given number of LUTs in a user circuit ("virtual LUTs") are reduced by a factor of the number of configurations.

Trimberger, col. 6, lns. 58-63. However, nothing in Trimberger teaches a logic computing unit providing "a logical function value of logic input data as logic output data, by referring to at least one configuration data module retrieved and stored in at least one of said plurality of data storage units *while another of said plurality of configuration data modules is being retrieved from outside the logic computing unit and stored in another one of said data storage units*," as recited in claims 1 and 11 of the present application. In fact, the present Office Action acknowledges that Trimberger does not teach how the programming of the logic circuits in his new FPGA is accomplished. (Office Action, page 7, ¶14).

As discussed in the present application, retrieving and storing multiple configuration data modules in corresponding data modules, such as a shift register, allows the logic computing unit (e.g., an FPGA) to continue computing data instead of sitting

idle and waiting for new configuration data to be retrieved from off-chip, and the reconfigure itself only after that data has been retrieved. Moreover, if the data modules do not contain the next needed configuration data, the system retrieves and stores that information while the logic unit continues with its computations. As a result, the claimed invention(s) provides for faster processing of large programs *with conventional logic circuits of an FPGA,* since the needed configuration data is already on-chip (i.e., within the system), and thus only hardware, rather than software, is employed during logic unit reconfiguration and computing. Because hardware is used in this manner over software, as is the case in conventional systems, the time required for shifting data modules is much shorter than the time required for writing to the data modules.

Trimberger does not provide the same advantages, and in fact requires the construction of an entirely new, and likely costly, FPGA to employ the teachings therein. Specifically, as cited above, Trimberger teaches creating a new FPGA having, in one embodiment, a bit set with 8 cells replacing each of the conventional 1 memory cells in a conventional FPGA. Thus, instead of providing multiple configuration data modules in a shift register for ready-use by the FPGA, Trimberger teaches the (re)configuration of 1 (or more) of the 8 cells in advance of that cell's use in computing. Moreover, the increase in logic density is provided by Trimberger at the expense of processing speed, resulting in a processing speed *even slower than conventional FPGAs*. Specifically, Trimberger provides for two reconfiguration methods, one based on an external signal and one done in continual cycles. However, both techniques have the FPGA sitting idle when awaiting reconfiguration:

> The chip waits doing no calculation (with low power consumption) until one of the selected set of input signals changes (i.e., goes high or low). At this point, the chip executes

> the reconfigurations associated with one major cycle (wherein a major cycle is a complete iteration through all reconfigurations), a fixed number of major cycles, or a number of major cycles or reconfigurations until an internal or external signal indicates a stop condition.

Trimberger, col. 18, lns. 14-18.

In sum, Trimberger teaches: (1) constructing multiple configuration memory cells in place of the conventionally used single memory cell, and then (2) configuring select ones of these memory cells that are not currently being used for computing in advance of their use in future logic computations. Accordingly, Trimberger is directed to increasing logic density by using multiple memory cells in place of single memory cells, typically at the expense of processing speed. (*See*, e.g., col. 22, lns. 62-64, and col. 23, lns. 65-67). In contrast, the present claims provide a logic system (and related method) *for use with a conventional logic computing unit* (such as a conventional FPGA's logic circuits having only single memory cells) for *faster processing than conventional FPGAs* of large programs. The faster processing is provided by the "behind-the-scenes" (i.e., while the logic circuits of the FPGA are computing) retrieving and storing of future-needed configuration data from off-chip data stores into on-chip data modules that are quickly and directly accessible by the FPGA hardware when reconfiguration of the conventional logic circuit is needed for continued program execution. Thus, the need for greater logic density is decreased because of the increased processing speed capable from the conventional logic circuits in the logic computing unit. Accordingly, Trimberger does not anticipate independent claims 1 and 11, as herein amended, and this rejection is respectfully requested to be withdrawn.

III. REJECTIONS UNDER 35 U.S.C §103

The Office Action has rejected dependent claims 2 and 12 under 35 U.S.C §103(a)

as allegedly obvious and thus unpatentable over Trimberger in view of U.S. Patent 5,036,473 to Butts *et al.* In addition, the Office Action has rejected dependent claims 3 and 13 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of Butts, and further in view of article drafted by Liu *et al.* Next, the Office Action has rejected dependent claims 5 and 15 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of the Liu article. Also, the Office Action has rejected dependent claims 8 and 18 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of the article drafted by Patterson *et al.*

The Applicants respectfully assert that all of these dependent claims are not obvious over the cited combinations of references. As discussed above, Trimberger does not teach or suggest all of the elements recited in independent claims 1 and 11, as amended herein. Moreover, Butts, Liu, and Patterson do nothing to cure the deficiencies of Trimberger discussed above, and is only relied upon for teaching specific limitation set forth in these rejected dependent claims. Specifically, these secondary references are offered for the teaching of shift registers for holding configuration data (Butts), the circular shift of the data in the shift register (Liu), selecting configuration data from the shift register (Liu), and selecting from the shift register based on a call signal (Patterson). However, even assuming these elements are taught by these secondary references as set forth in the Office Action, the cited combinations still do not teach a logic computing unit providing "a logical function value of logic input data as logic output data, by referring to at least one configuration data module retrieved and stored in at least one of said plurality of data storage units *while another of said plurality of configuration data modules is being retrieved from outside the logic computing unit and stored in another one of said*

data storage units," as recited in claims 1 and 11 of the present application.

As a result, the combinations of Trimberger with Butts, Liu, and Patterson, or various combinations thereof, still do not teach or suggest all of the elements of independent claims 1 and 11. Since dependent claims 2 and 12, 3 and 13, 5 and 15, and 8-18 depend from independent claims 1 and 11, respectively, these dependent claims are also not obvious in view of the various cited combinations of references set forth in the rejections. Accordingly, the Applicants respectfully request that the Examiner also withdraw the §103(a) rejections with respect to the pending claims.

IV. CONCLUSION

The Applicants respectfully submit that the pending claims are in condition for allowance, and request a Notice of Allowability for the pending claims. The Examiner is invited to contact the undersigned Attorney of Record if such would expedite the prosecution of the present Application. The three-month response deadline expired on November 15, 2006. Thus, this Amendment is being filed with a two-month Request for Extension of Time, along with the required fee, to extend the respond period to January 16, 2007 (since January 15, 2007, fell on a federal holiday). Accordingly, this Amendment is timely. If further fees are believed due, or an overpayment has occurred, the Director is authorized to charge or deposit any necessary fees to Deposit Account No. 13-0480.

Respectfully submitted,

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